An Efficient Computational Method for Modeling Interface Roughness in Laterally Contacting Tri-Metal Double Gate MOSFETs

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ABSTRACT

A computational method for modelling the effects of interface roughness in the high-κ, Laterally Contacting Tri-Metal Double Gate MOSFET(LCTM DGMOSFET), which is a structural modification of the normal Double Gate MOSFET(DGMOSFET) is presented. It is assumed that the interface roughness is due to the fluctuation of the oxide thickness from its average value. The transport equation and the boundary conditions appropriate for the rough surface are discussed. The computational method consists of solving the Non Equilibrium Green's Function(NEGF) equations coupled with the Poisson's equation in a self-consistent manner. The effect of energy dissipation due to scattering at the rough surface is incorporated by the introduction of Buttiker probes along the transport direction. Different gate dielectric materials--SiO_2, Si_3N_4, $HfSiO_4$, Y_2O_3, and Ta_2O_5-- are used in different structures to investigate the effect of high-κ gate materials. The metals Ta, TaSiN and Al are used to form gate combinations Ta-Al-Ta, TaSiN-Al-TaSiN and Al-Al-Al. It is found that the device characteristics such as the threshold voltage and the subthreshold swing vary appreciably from the ideal value due to the presence of roughness at the interface, and that the roughness points near the control gate where the oxide layer protrudes into the Si channel cause the largest variation in device parameters from the smooth ideal interface value. The results confirm that LCTM DG MOSFETs possess better immunity to fluctuations arising from interface roughness when compared with normal DG MOSFET with the same degree of roughness.

INTRODUCTION

As the process of device downscaling is approaching its final phase[1], the fundamental problem faced by the semiconductor industry is the fact that semiconductor designs have some amount of fluctuations as devices become smaller. The innate randomness of these device designs produce changes in each device resulting in an ensemble of devices with varying device characteristics, and the assumption that each device in an IC is identical is no longer valid. These device geometry fluctuations include line edge roughness (LER), random dopant distribution, and interface roughness (surface roughness). Interface roughness is the presence of imperfections in the atomic boundary between the channel and the oxide layer. These imperfections arise due to the inability of the manufacturing processes to precisely position oxide atoms and semiconductor atoms in the oxide/channel interface layer at scaled dimensions. DGMOSFETs, unlike bulk MOSFETs, have two interfaces and therefore the

effects of any interface roughness in the Si/SiO_2 boundary will be magnified. For instance, in an Ultra Thin Body (UTB) DG MOSFET, interface roughness not only affects the thickness of the channel, but changes the oxide layer thickness too as depicted in figure 1(b). schematically.

In DG structures the charge density is maximum at the center of the channel where transverse fields are lower due to size quantization effects and volume inversion tend to concentrate the charge density in the center of the channel, resulting in a less pronounced interface scattering effects [2, 3]. However, due to the extremely thin channels, roughness of the surface results in an appreciable channel thickness fluctuation in such UTB devices. As a result, the potential profile gets distorted appreciably at these surface imperfections leading to altered transport characteristics. Thus, more than the scattering from imperfection potentials, scattering from potential fluctuations in the channel is the major concern in UTB DG MOSFETs. It has been shown experimentally and through numerical simulations that the electron mobility is degraded as the oxide thickness is reduced [4-7]. Therefore, quantification of the effects of surface roughness on device characteristics is necessary to fabricate devices in a chip that will function within the specified tolerance limits.

Among DG MOSFETs, which are being regarded as one of the best device structures to continue the process of device downscaling below 10nm, the structurally modified geometry in which parallel connected hetero-material double-gates and high- κ dielectric layers are employed possess superior subthreshold behavior and ballisticity[8, 9] that are required for future nanoscale devices as envisaged in the ITRS road map[1]. This paper attempts to analyze the effect of interface roughness on the device performance of such structurally modified DG MOSFET structures with parallel connected gates and high-κ oxide layers.

2 Interface Roughness Model of LCTM DG MOSFET

Numerical models to quantify roughness effects in devices usually rely on a power spectrum corresponding to the Gaussian or exponential autocorrelation function of the interface roughness to generate random channel/oxide and gate/oxide interfaces[10-13]. In this model, it is assumed that the interface roughness is due to the fluctuation of the oxide thickness T_{ox} from its average value $\bar{T}_{ox}$, according to figure 1(b). So, at a given position x, in the plane parallel to the gate, the oxide thickness is given by

$$T_{ox}(x) = \bar{T}_{ox} + \Delta(x) \qquad 1$$

where $\Delta(x)$ is the oxide thickness deviations from its average value, which are assumed to be correlated. This correlation is measured by the autocorrelation function, which is assumed to follow a Gaussian or exponential law [11,12].

Interface roughness generation for the devices involves combining a chosen power spectrum with associated randomized phases. This is done by setting up a complex vector, A(n), in 1-D, which has amplitude terms determined from the spectral function, while random phase elements are assigned with conjugate symmetry condition (A(i) = A*(N-i)). The inverse Fourier Transform is then taken to construct rough lines that have both a controlled element (the power spectrum) and a random element (the phases). The end result is randomized lines that have a given correlation length and RMS value. The devices simulated in this study are 2D, so only 1D rough lines are required.

Given the type of power spectrum (exponential or Gaussian), correlation length, and RMS parameter, the power spectrum is given by the equations[14]:

$$S_G = \sqrt{\pi}\Delta^2\Lambda e^{-\frac{q^2\Lambda^2}{4}} \quad \textbf{2}$$

$$S_E = \frac{2\Delta^2\Lambda}{1+q^2\Lambda^2} \quad \textbf{3}$$

S_G and S_E are the power spectrums of the Gaussian and exponential roughness. The correlation length Λ is a measure of the distance between points on the rough line that have similar magnitudes. The RMS value Δ corresponds to the root-mean-square of the final roughness. This allows the magnitude of the rough line to be set to correspond to 1 atomic step of Silicon (0.3 nm) in these simulations. The independent variable q corresponds to the location along the rough line.

3 Transport Equation and Boundary Conditions for the Rough Surface

The self-consistent simulation loop to obtain transport characteristics of the device consists of two blocks: the Poisson equation which is solved for the potential profile and the Non Equilibrium Green's Function (NEGF) transport equation which is solved for charge and current distribution in the device. The finite difference discretization scheme is used for the numerical implementation of both of these blocks [15, 16]. In figure 1(b) we show the simulation domain and grid mesh used for the numerical modeling of the model device, the LCTM DG MOSFET, that we have chosen for demonstration. The finite difference grid consists of uniformly spaced nodes with a mesh spacing of *a* along the transport direction *x* and *b* along the confinement direction *y*. The simulation domain of the self-consistent loop includes the S/D extension regions, the channel and the top and bottom oxide layers.

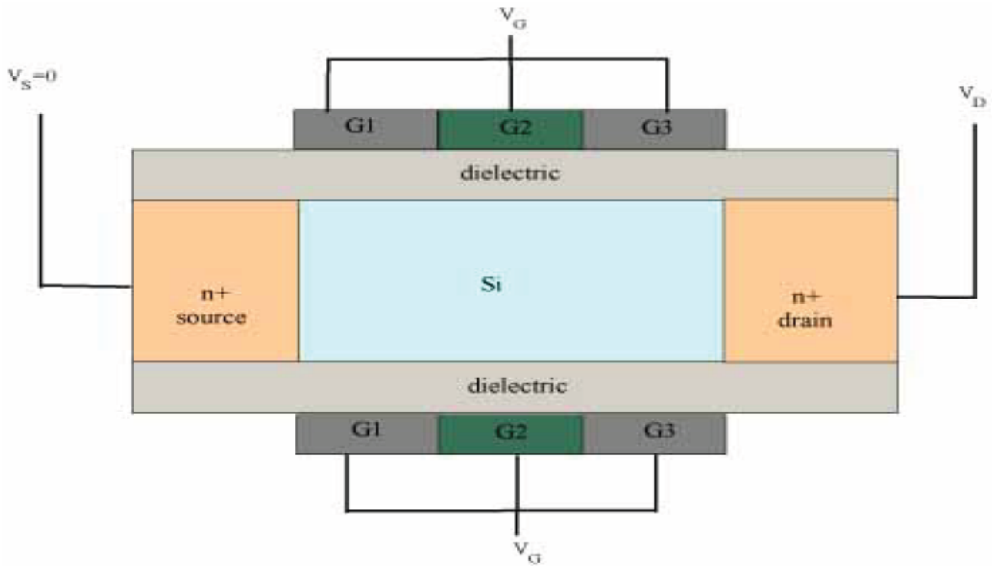

Figure 1 (a): DG MOSFET with parallel connected gates with smooth interface layer

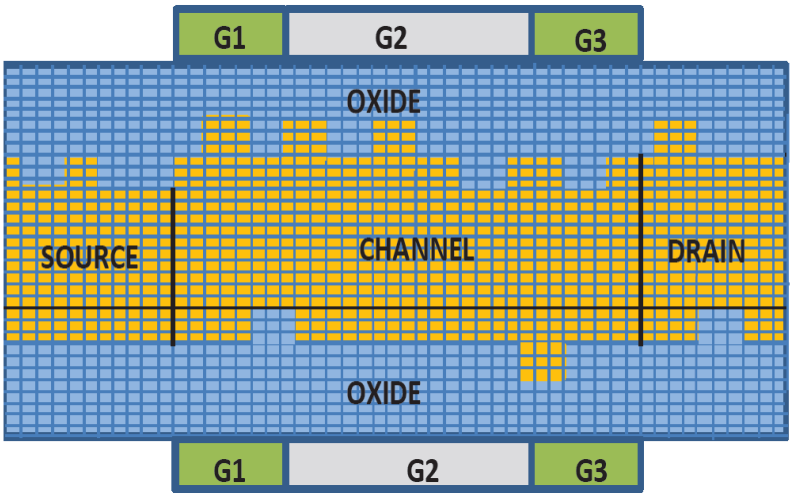

Figure 1(b): LCTM DG MOSFET with channel discretization of one of the simulated cases of surface roughness.

A 2D numerical solution to the Poisson's equation

$$\nabla.(\epsilon \nabla U_{SC}) = -q^2(p - n + N_D - N_A)$$

is composed of potential values at each lattice node of the finite difference grid shown in figure 1(b). To attain these $N_X . N_Y$ potential values, the necessary equations are obtained by applying equation 4 at all internal nodes of the simulation grid and boundary conditions at the Si/oxide interface nodes. At any internal node (m,n), equation 4 takes the form,

$$\frac{a}{b}V_{m-1,n} + \frac{b}{a}V_{m,n-1} - 2\left(\frac{a}{b}+\frac{b}{a}\right)V_{m,n} + \frac{b}{a}V_{m,n+1} + \frac{a}{b}V_{m+1,n} = -\frac{ab}{\epsilon}q(N_D - N_A - n)_{m,n} \quad \textbf{(a)}$$

In the case that the node is positioned at the Si/Oxide interfaces, equation 4 has the form

$$\frac{a}{b}V_{m-1,n} + \left(\frac{b}{2a}\right)\left(1+\frac{\epsilon_{BOT}}{\epsilon_{TOP}}\right)V_{m,n-1} - \left(\frac{a}{b}+\frac{b}{a}\right)\left(1+\frac{\epsilon_{BOT}}{\epsilon_{TOP}}\right)V_{m,n} + \left(\frac{b}{2a}\right)\left(1+\frac{\epsilon_{BOT}}{\epsilon_{TOP}}\right)V_{m,n+1} + \frac{a}{b}\left(\frac{\epsilon_{BOT}}{\epsilon_{TOP}}\right)V_{m,n+1} = -\frac{ab}{\epsilon_{TOP}}q(N_D - N_A - n)_{m,n} \quad \textbf{(b)}$$

At the nodes on the upper and lower oxide/semiconductor interface where roughness occurs (nodes numbered 1 through 10 in figure 2(b)), equation 4 takes the following form

$$\left(\frac{a}{2b}-\frac{b}{8a}\right)(\epsilon_{tl}+\epsilon_{tr})U_{SC}(m-1,n)+\left(\frac{b}{8a}\right)(\epsilon_{tr})U_{SC}(m-1,n+1)$$
$$+\left(\frac{b}{8a}\right)(\epsilon_{tl})U_{SC}(m-1,n-1)$$
$$-\left(\frac{a}{2b}+\frac{3b}{8a}\right)(\epsilon_{tl}+\epsilon_{tr}+\epsilon_{bl}+\epsilon_{br})U_{SC}(m,n)$$
$$+\left(\frac{a}{2b}-\frac{b}{8a}\right)(\epsilon_{bl}+\epsilon_{br})U_{SC}(m+1,n)+\left(\frac{b}{8a}\right)(\epsilon_{bl})U_{SC}(m+1,n-1)$$
$$+\left(\frac{b}{8a}\right)(\epsilon_{br})U_{SC}(m+1,n+1)+\left(\frac{3b}{8a}\right)(\epsilon_{tr}+\epsilon_{br})U_{SC}(m,n+1)$$
$$+\left(\frac{3b}{8a}\right)(\epsilon_{tl}+\epsilon_{bl})U_{SC}(m,n-1)=-(abq^2)(N_D-N_A-n)_{m,n} \quad \textbf{(c)}$$

where $\epsilon_{tl}, \epsilon_{tr}, \epsilon_{bl}, \epsilon_{br}$ are the dielectric constants of the material around the node (m,n) as shown in figure 2(a). At the gate contacts, Dirichlet boundary conditions are used. Thus,

$$U_{G_j} = -V_{G_j} + \Phi_{M_j} - \Psi_{Si} \quad \textbf{(d)}$$

where V_{G_j} is the gate bias at the gate G_j, Φ_{M_j} is the work function of the metal forming the gate G_j, and Ψ_{Si} is the electron affinity in the silicon channel. Neumann boundary conditions

$$\vec{n}.\nabla V = 0 \quad \textbf{(e)}$$

are imposed at the source/drain contacts and at other boundaries without electrode contacts.

Roughness modifies the subband energy profile inside the channel and the carriers encounter a changing energy band landscape along the channel of the device as they propagate from source to drain. Energy relaxing scattering process occur with greater probability due to these potential bumps leading to a substantial decrease in the mobility and hence the drain current. The energy relaxed probe model concept [17] of the Buttiker model[18], in which the probes placed at every node along the transport direction act as reservoirs extracting electrons from the device, perturbing the energy and momentum of those electrons and re-injecting them back into the system with a different energy and momentum distribution is suitable to find the combined effect of all such scattering events arising due to the surface imperfections. The net current at any probe including contributions from all other probes *n*, all modes *m* and valleys *i* is given by

$$I_m(E_l) = \frac{q}{\hbar^2}\sqrt{\frac{m_{ti}^* k_B T}{2\pi^3}}\sum_n \left[\mathcal{F}_{-1/2}(\mu_m - E_l) - \mathcal{F}_{-1/2}(\mu_n - E_l)\right].T_{mn}$$

where E_l is the longitudinal energy of the carrier in the transport direction, m_{ti}^* is the electron effective mass transverse direction for the valley *i*, $\mathcal{F}_{-1/2}$ is the Fermi integral of order -1/2 and μ_n is the probe potential. T_{mn} is the transmission given by

$$T_{mn}(E_l) = \Gamma_m |G_{mn}|^2 \Gamma_n$$

where $\Gamma_{m,n}$ are the perturbation strengths of the probes and G_{mn} is the Green's function.

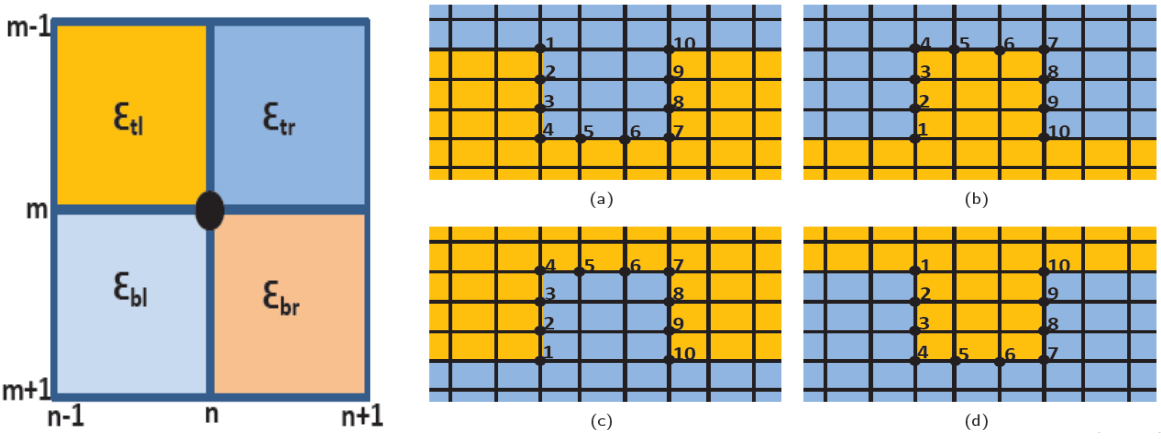

Figure 2: (a) The general distribution of dielectric constant about the node (*m,n*) located along oxide/semiconductor interface used in the calculation of equation 4. (b)Node numbering to model surface roughness in LCTM DG MOSFETs due to the projection of oxide layer and Si channel into one another at the top and bottom interfaces

The coupling energy of every probe is dependent on the subband energy at the point on which the probe is located. Therefore, probes characteristics take into account the change of the energy levels due to roughness-induced oxide variations, necessitating the introduction of no additional scattering factor to account for the interface roughness [14].

4 Method of Simulation

Figure 1(a) and 1(b) show the simulated LCTM DG MOSFET with parallel connected gates of different gate materials with a channel length of 10nm and channel thickness of 3nm. The device has heavily n-doped (N_D=10^{20} cm^{-3}) source and drain regions. The top and bottom gates of the MOSFET consist of three laterally contacting metals of different work functions, with a narrow dielectric diffusion layer between them. The parallel combination of the gates $G_1G_2G_3$ forms the top and bottom gates. Different gate dielectric materials- SiO_2, Si_3N_4, $HfSiO_4$, Y_2O_3, and Ta_2O_5-were used in different structures to investigate the effect of high-κ gate materials. The metals Ta, TaSiN and Al were used to form gate combinations such as Ta-Al-Ta, TaSiN-Al-TaSiN, Al-Al-Al etc. The source and drain extension regions were 4nm and the average physical thickness of the insulator layer was kept at 1nm. We assumed a Gaussian roughness with the correlation length Λ varying from 6nm to 12nm and an RMS value of 0.3nm suitable for the Si lattice. An ensemble of 50

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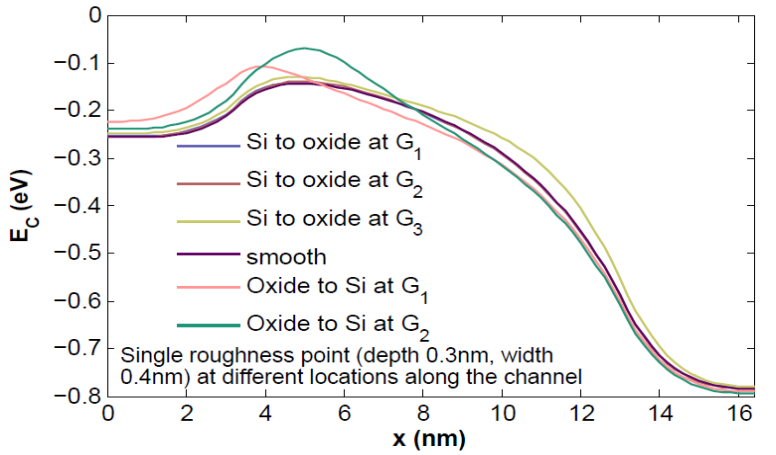
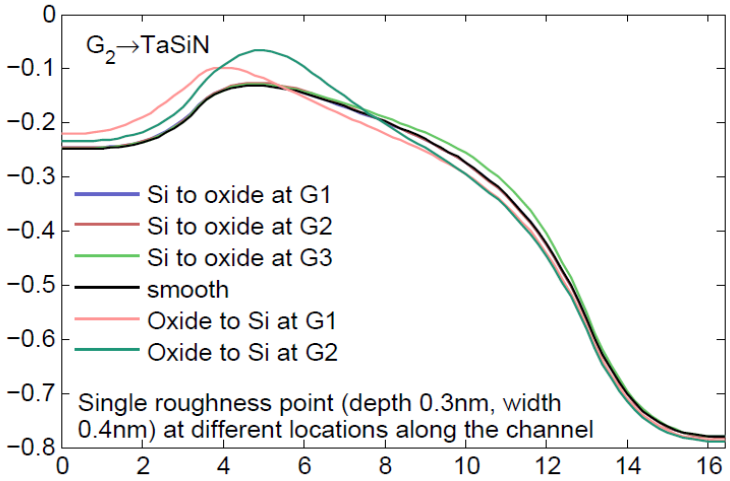
devices with a given κ and random roughness were simulated to get the average effect of roughness.

5 Results and Discussion

Figure 3 shows the potential profile variations due to the body thickness fluctuation associated with the rough interfaces. For comparison, in the figure we have included the potential profile of devices with smooth interfaces (shown in figure 1(a)) also. Figures 3(a) and 3(b) show the potential through the center of the channel along the transport direction *x* for Al-Al-Al and TaSiN-Al-TaSiN devices respectively.



(a)



(b)

Figure 3: Conduction band edge profile (a) along the transport direction for a DG MOSFET having Al gates with one roughness point at different locations along the channel (b) along the transport direction for a LCTM DG MOSFET having TaSiN-Al-TaSiN gates with one roughness point at different locations along the channel

The height of the barrier is significantly altered from the ideal smooth value for both devices. The shift in the profile is most marked for a roughness point at G_2 where the oxide layer projects into the Si channel. Figure 4 shows the variation in potential for these devices along the confinement direction y through the roughness point located at G_2. The TaSiN-Al-TaSiN device shows a largest bump in the potential at the interface layer where the oxide layer projects into the channel.

The modification in the potential profile causes fluctuations in the electron density and alters the device characteristics significantly. Figure 5 shows the variation in electron concentration due to the body thickness fluctuation associated with the rough interfaces. Figure 5(a) and figure 5(b) show the charge concentration in the channel for the smooth Si/Ta_2O_5 interface LCTM DG MOSFETs with Al gates and parallel connected TaSiN-Al-TaSiN gates respectively. Figure 5(c) and figure 5(d) show the electron concentration in the channel for the same devices, but with the Si layer protruding into the upper SiO_2/Ta_2O_5 layer below the left screen gate G_1. The roughness alters the electron density at the location of the roughness with a marked carrier penetration into the oxide at the roughness point and an accompanying decrease in the electron density near the lower interface region. The high-κ Al gate LCTM DG MOSFET and the high-κ parallel connected TaSiN-Al-TaSiN gate LCTM DG MOSFET show this carrier penetration, but the effect is less significant in high-κ parallel connected TaSiN-Al- TaSiN gate LCTM DG MOSFET due to the better electrostatic immunity offered by the high workfunction of the TaSiN screen gate. Figure 5(e) and figure 5(f) show the electron concentration in the channel for high-κ Al gate DG MOSFET and the high-κ parallel connected TaSiN-Al-TaSiN gate LCTM DG MOSFET with identical randomly generated upper and lower rough interfaces. It is clear that roughness produces strong variations in the electron concentration in the channel for both devices and makes the current path longer compared to the smooth interface case. For the smooth device, the electron density is largest at the middle of the channel along the transport direction. However, for rough devices, this need not be the case as evident from figures 5 (e) and 5(f) where the electrons are pushed towards the interface layers causing significant increase in the probability of scattering from interface potential wells.

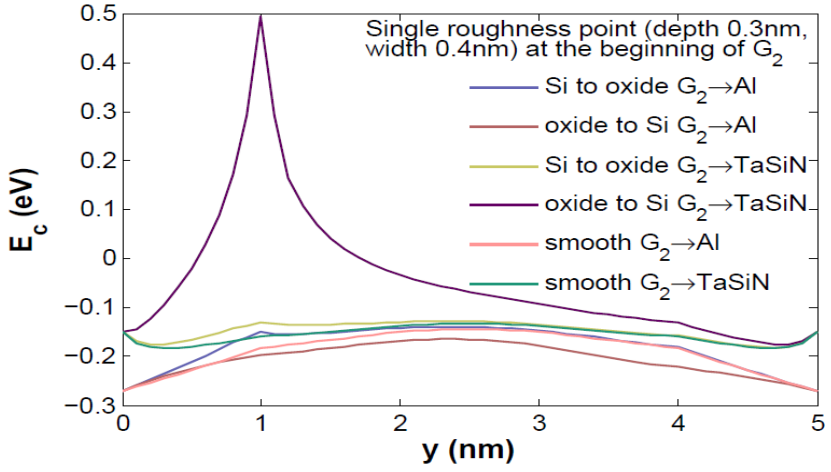
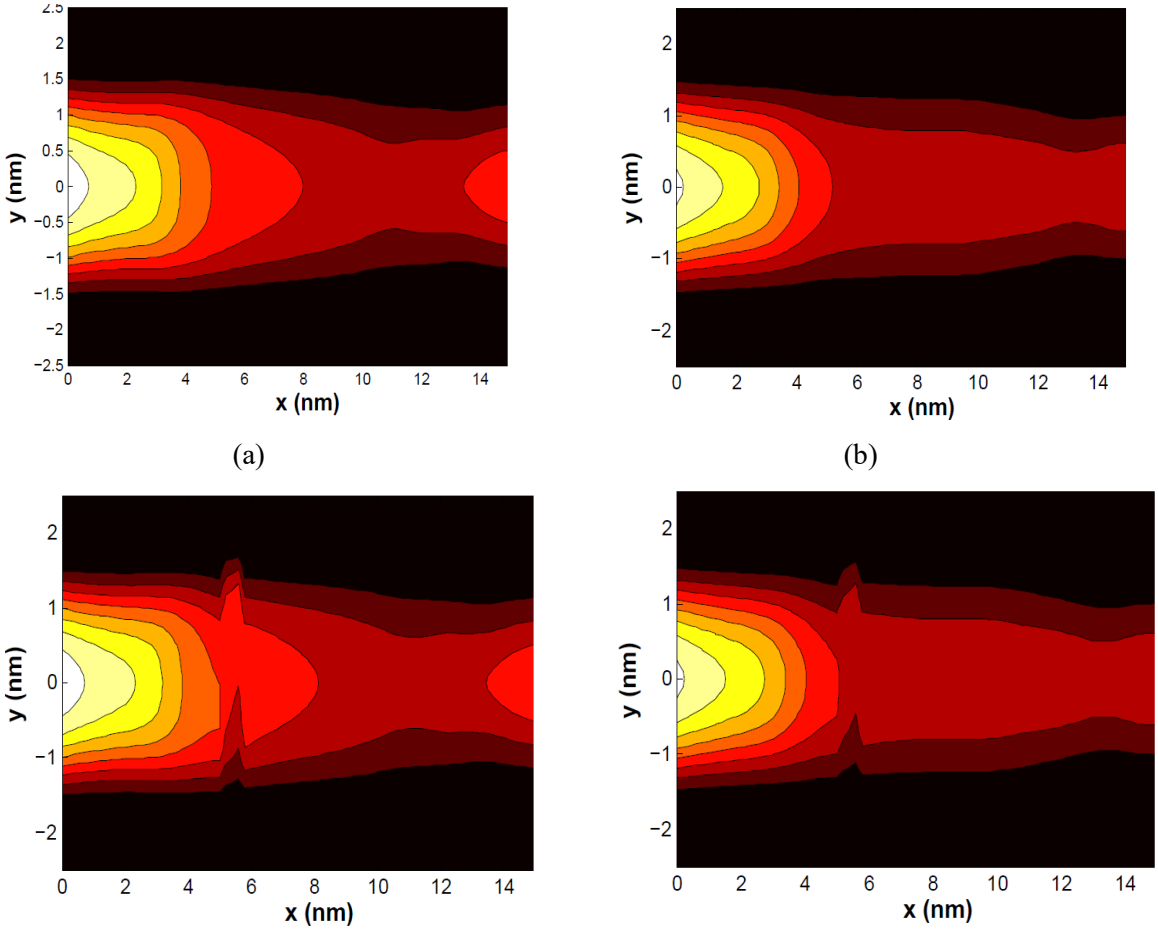


Figure 4: Conduction band edge profile along the confinement direction through the roughness

point (G_2) for devices having Al gates and TaSiN-Al-TaSiN gates with one roughness point.

The electron density of LCTM DG MOSFET with high-κ oxide layers along the transport and confinement directions with one rough point at the interface are shown in figure 6. Figure 6(a) compares the electron density along the confinement direction through the roughness point (located below the middle gate G_2) for gate combinations TaSiN-Al-TaSiN, Ta-Al-Ta and Al-Al-Al with that of the smooth devices. The electron density near the rough interface shows an increase from its value at the smooth interface for all gate combinations. This increase is more marked for devices with low work function screen gates. This increase in electron density near the interface should produce a proportionate increase in the scattering of electrons by potential wells at the roughness points.

However, as evident from figure 6(c), at a roughness point where the oxide layer penetrates into the semiconducting channel the electrons are pushed away from the interface



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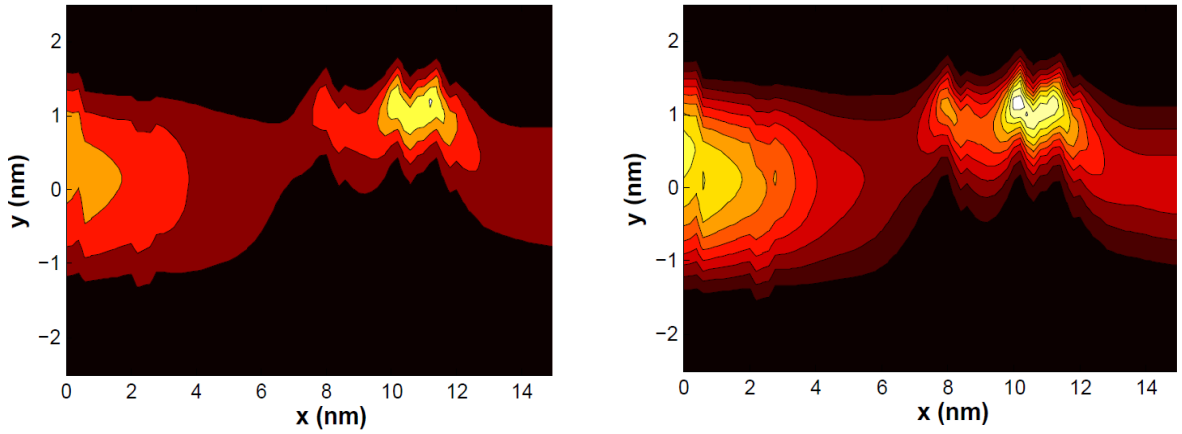

(e) (f)

Figure 5: 2D electron density profile inhomogeneity due to a single interface roughness point (a) DG MOSFET with Al gates having no roughness (b) LCTM DG MOSFET with TaSiN-Al-TaSiN gates having no roughness (c) DG MOSFET having Al gates with the Si channel projects into the oxide layer at the upper middle gate G_2 (d) LCTM DG MOSFET having TaSiN-Al-TaSiN gates with the Si channel projects into the oxide layer at the upper middle gate G_2 location (e) DG MOSFET with Al gates having a random rough interface (f)LCTM DG MOSFET with TaSiN-Al-TaSiN gates having a random rough interface.

more into the interior of the channel leading to a reduction in the rate of scattering by surface roughness potential wells. These two effects, the increase of electron density at the interface at points where the channel protrudes into the oxide layer and the decrease of the electron density at points where the oxide layer projects into the channel, roughly cancels out in a device and the average effect is same as that for a normal DG MOSFET where the scattering by roughness points are negligible because most of the electrons are concentrated at the center of the channel due to quantum confinement. The effect of roughness in DG MOSFETs therefore reduces to the scattering of electrons arising from the fluctuations in the potential profile due to body thickness variation of the channel.

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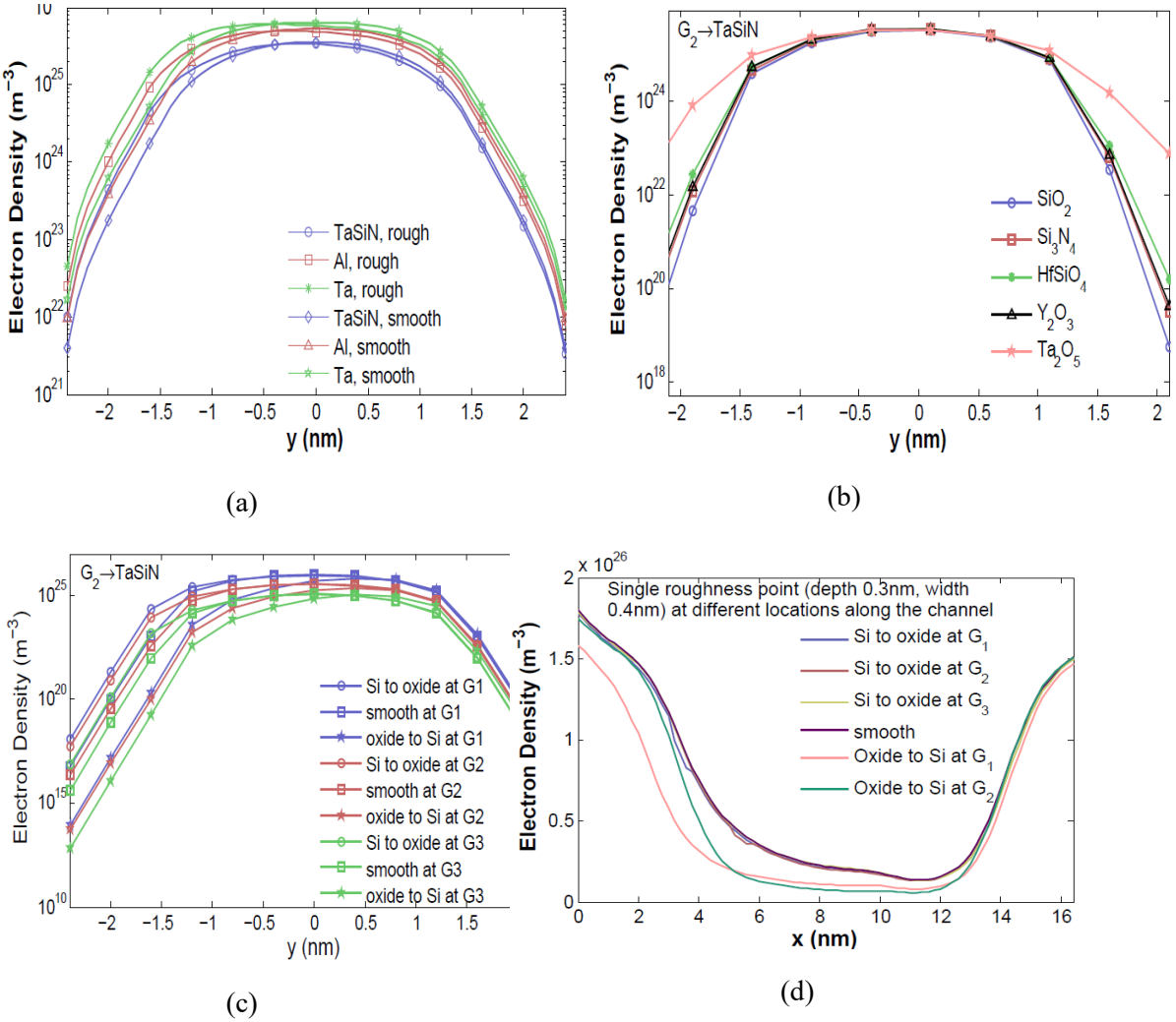

Figure 6: Electron concentration along (a) confinement direction through the roughness point G_2 for LCTM DG MOSFET having various gate combinations (b) confinement direction through the roughness point G_2 for TaSiN-Al-TaSiN device having different high- κ dielectric layers (c) confinement direction through the roughness point G_1, G_2 and G_3 for TaSiN-Al-TaSiN device having Ta_2O_5 dielectric layer (d) transport direction for Al-Al-Al, SiO_2 device having one roughness point at G_1, G_2 and G_3

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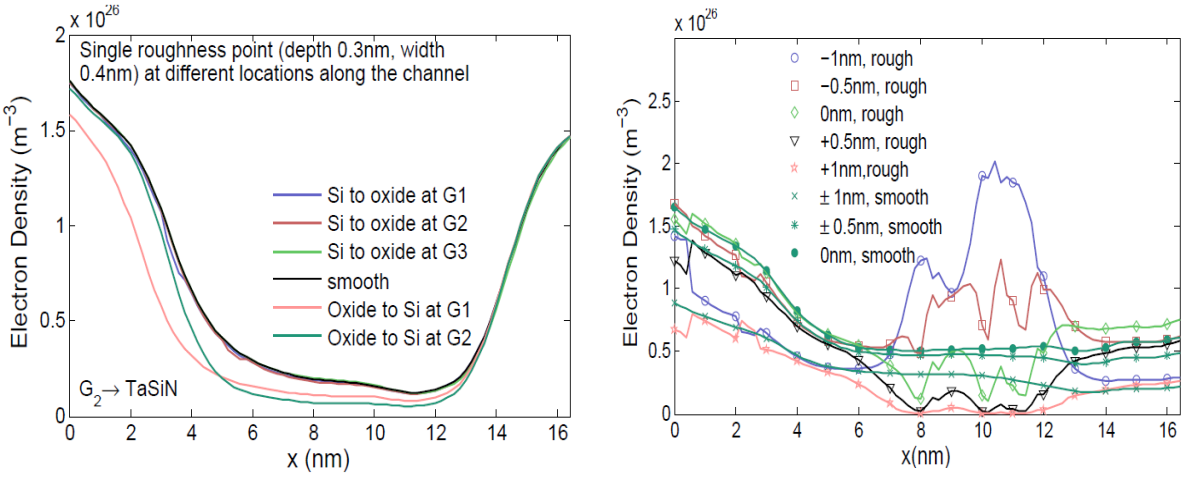
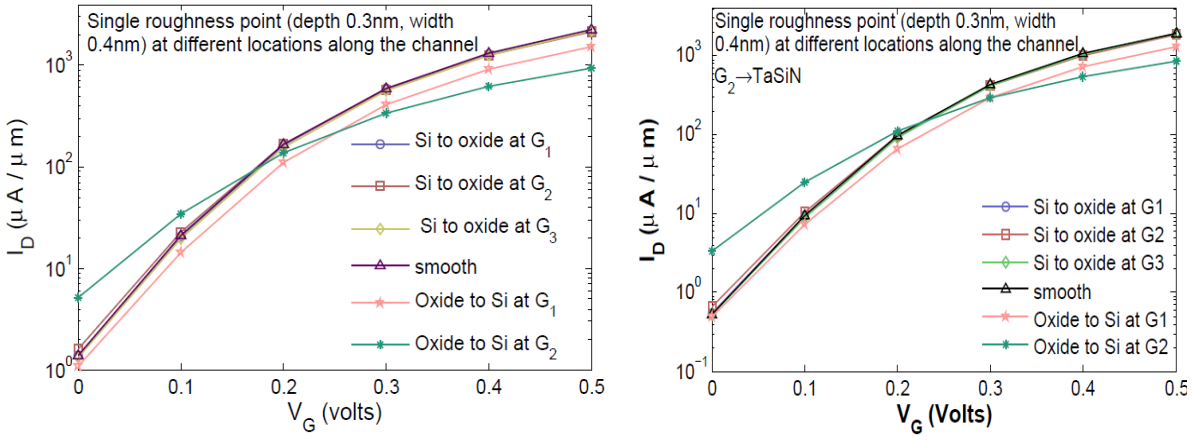


Figure 7: Electron concentration along (a) transport direction for TaSiN-Al-TaSiN, SiO2 device having one roughness point at G1, G2 and G3 (b) channel at different distances from the middle of the channel for TaSiN-Al-TaSiN, Ta2O5 device having random roughness.



(a) (b)

Figure 8: Gate characteristics of DG MOSFET with (a) Al gates having a single roughness point at different locations along the channel (b) TaSiN-Al-TaSiN gates having a single roughness point at different locations along the channel

Figure 6(b) shows the electron density along the confinement direction through the roughness point at G_2 for the TaSiN-Al- TaSiN parallel connected gate DG MOSFET with different oxide layers. An increase in κ of the oxide layer increases the electron density near the interface if Si steps into the oxide layer at the interface. The effect is largest for the Ta_2O_5 layer, indicating more electron penetration into the oxide layer at the point of roughness. As described before, a roughness point where the oxide projects into the channel has a correspondingly larger decrease of electron density at the interface for the Ta_2O_5 layer causing no marked increase in the scattering from potential wells at the roughness points.

Figure 6(c) shows that the roughness point at the interface near the beginning of the control (middle) gate G_2 has the largest effect in distorting the symmetric nature of the electron

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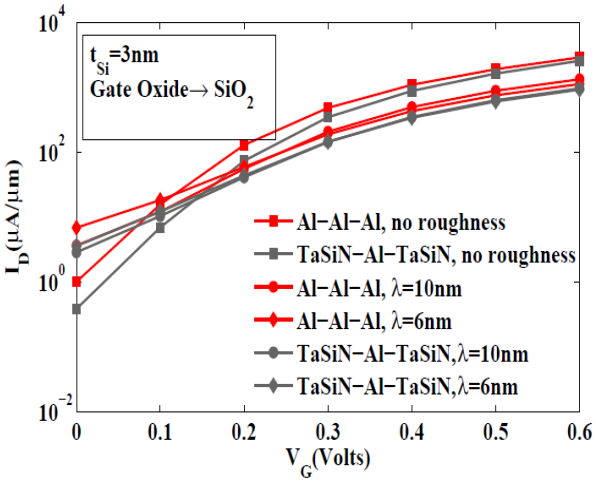
density profile of the DG MOSFET with a smooth interface. Figures 6(d) and 7(a) show the variation of the electron density along the transport direction at the center of the channel (where the charge concentration is largest) for Al-Al-Al and TaSiN-Al-TaSiN devices having SiO_2 layer. A roughness point where the oxide penetrates into the Si channel has a significant reduction in the electron density at the center of the channel from the ideal smooth device value for both device structures. Fluctuation in electron concentration along the transport direction at different distances from the middle of the channel (y = 0:0 denotes the middle of the channel) is presented in figure 7(b) for a TaSiN-Al- TaSiN device with randomly generated rough surface. It shows that the electron density near the rough interface may be many orders of magnitude greater than that at the middle of the channel.



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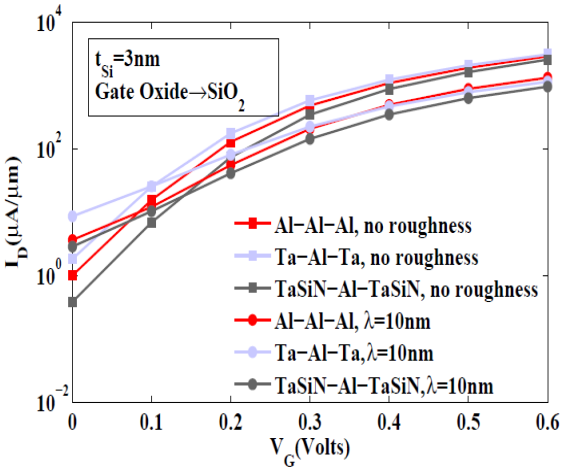

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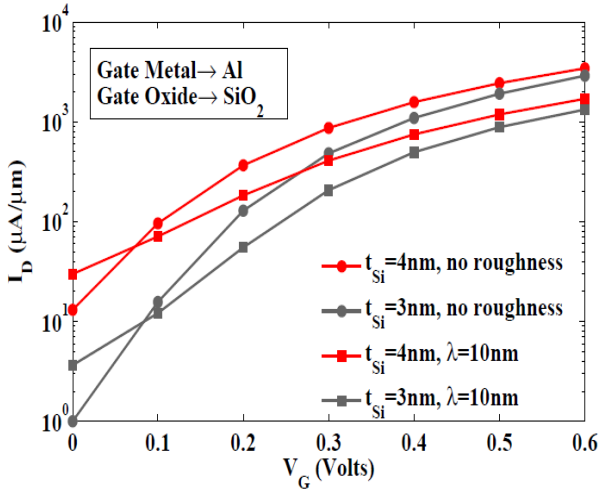
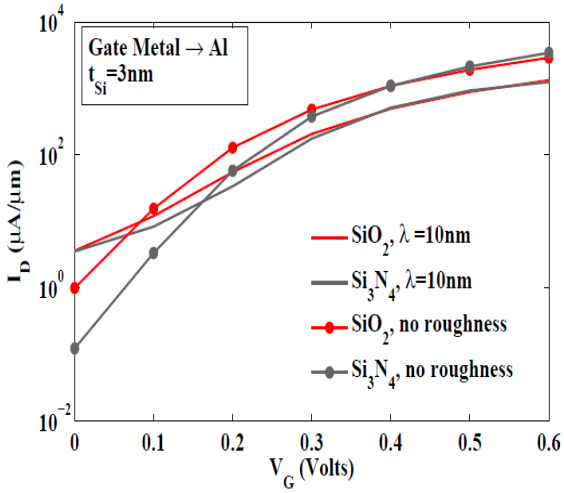


(c)



(d)

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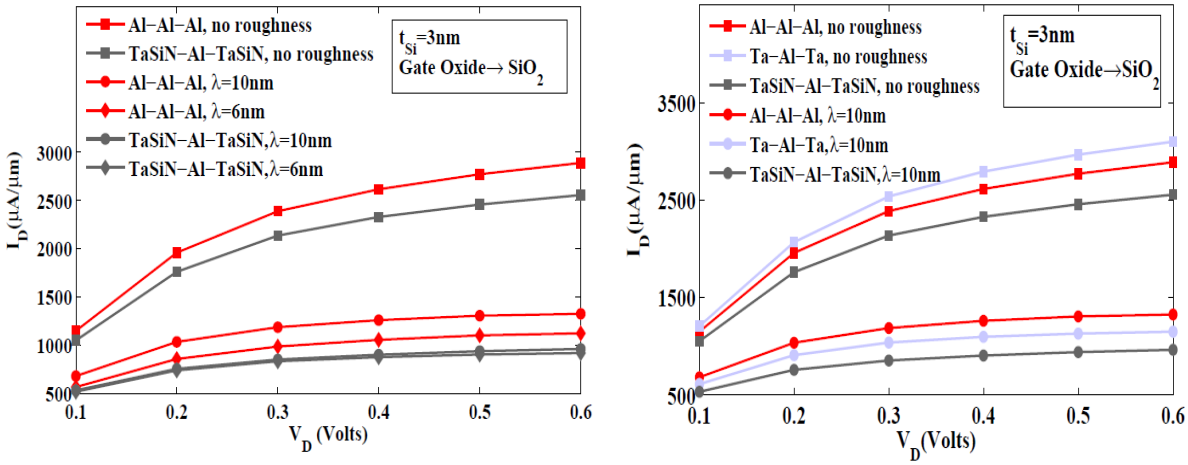
Figure 9: Gate characteristics of DG MOSFET with (a) randomly generated rough surfaces having different correlation lengths (b) randomly generated rough surfaces having different gate metal combinations (c) randomly generated rough interfaces having different channel thickness and (d) randomly generated rough surface having different oxide layers.

Fluctuations in electron density cause the device characteristics to vary significantly among rough devices. Figures 8 and 9 show the variations in gate characteristics for devices of different gate combinations and oxide layers with rough surfaces of various correlation lengths. The effect of roughness points located at different positions on the channel along the transport direction for a normal gate device and parallel connected TaSiN-Al-TaSiN device are shown in figures 8 (a) and 8 (b) respectively. Roughness causes the off-state leakage current to increase identically in both device structures. The degradation of the subthreshold behavior is most significant when the oxide layer projects into the channel at the interface below the control gate G_2 while for other cases it is less significant and is close the ideal interface situation. When the oxide layer projects into the channel at the interface below the screen gate G_1, the leakage current is close to the ideal surface case for the TaSiN-Al-TaSiN device owing to the better electrostatic integrity provided by the high workfunction gate metal. The saturation current is also significantly reduced from the ideal surface value when the oxide layer projects into the channel at G_2. However, comparing figures 8(a) and 8(b), it is clear that the degradation of the I_{on} / I_{off} ratio is less for the TaSiN-Al-TaSiN device than that for the normal Al gate device.



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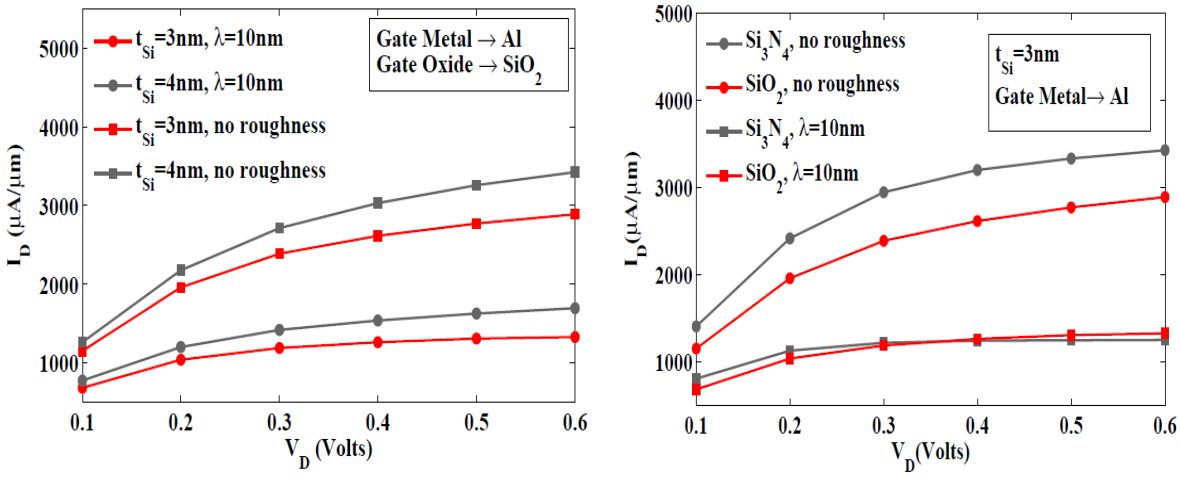
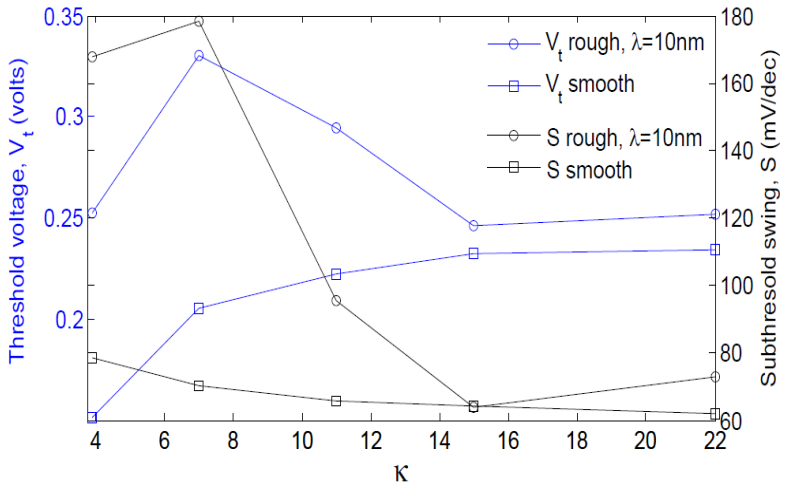


Figure 10: Comparison of ensemble average of drain characteristics of devices (a) with randomly generated rough surfaces of different correlation lengths for parallel connected gates and normal gates (b) with randomly generated rough surfaces for parallel connected gates of different metal combinations (c) with randomly generated rough surfaces of different channel thickness and (d) rough device with different oxide layers.

Figures 9(a) and 9(b) compare the gate characteristics of parallel connected TaSiN-Al-TaSiN and Ta-Al-Ta devices having randomly generated rough surfaces of different correlation lengths with normal devices having ideal interfaces. A smaller correlation length produces a larger deviation from the ideal value as expected for rougher surfaces. However, the high workfunction of the screen gate shields the device from such fluctuations to some extent in parallel connected gate devices. Thus the device with Ta-Al-Ta suffers the severest degradation due to the random nature of the surface imperfections, whereas the LCTM device with high workfunction metal TaSiN as the screen gate contact has the best immunity to subthreshold degradation of all the devices that we analyzed in the work.



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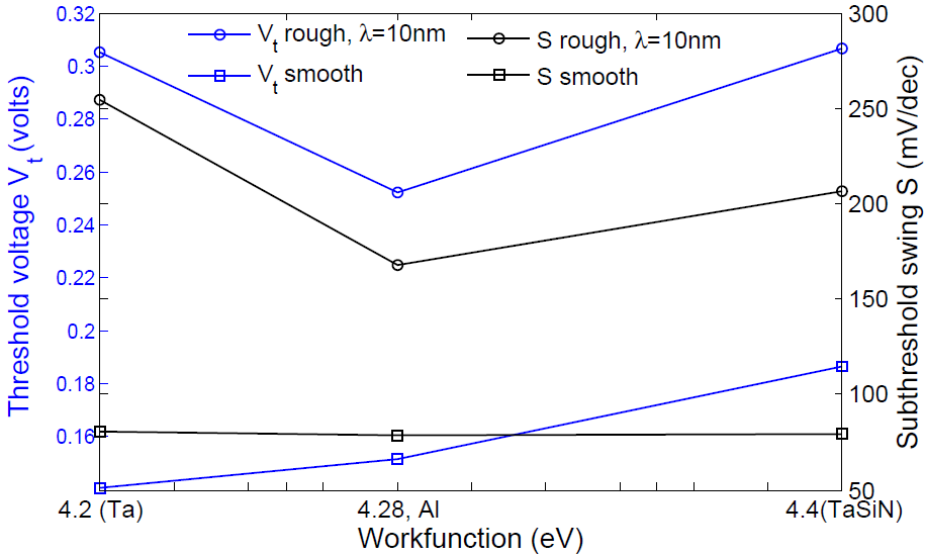
(a)



(b)

Figure 11: Variation of the ensemble averaged threshold voltage Vt and subthreshold swings with (a) dielectric constant of the gate oxide layer and (b) workfunction of the gate contact metal for high-κ devices having random roughness

Figures 9(c) and 9(d) show the subthreshold behavior of DG MOSFETs with different channel thickness and different oxide layers. From figure 9(c) it is clear that the subthreshold performance of the device with rough interfaces deviates more from the ideal device for thinner channels indicating that surface roughness is one of the most important problems to be addressed at the design phase while devices are downscaled. Figure 9(d) compares the subthreshold behavior of the normal device having SiO_2 layer with that of a normal device having high-κ layer Si_3N_4. The subthreshold degradation due to roughness aggravates as the dielectric constant of the oxide layer increases. Thus, even though high-κ oxide layers are necessary to suppress gate leakage currents during downscaling, they cause the roughness induced subthreshold leakage to increase. To reduce this roughness induced leakage with increasing dielectric constant in normal Al gate DG MOSFET, a LCTM DG MOSFET such as TaSiN-Al-TaSiN is needed.

The comparison of ensemble averaged drain characteristics of devices having randomly generated rough surfaces with the characteristics of ideal smooth interface devices is shown in figure 10. Figure 10(a) shows the drain current variation of TaSiN-Al-TaSiN parallel connected gate device and normal Al gate device having randomly generated rough interface of correlation lengths 6 nm and 10 nm. For the normal Al gate device the ensemble averaged saturation current drops by 61% and 54% respectively for correlation lengths 6 nm and 10 nm. For the TaSiN-Al-TaSiN parallel connected gate device the ensemble averaged saturation current drops by 63% and 62% respectively for correlation lengths 6 nm and 10 nm. The average deviation for the TaSiN-Al-TaSiN parallel connected gate device is not

better than that for the normal Al gate device unless a high-κ oxide layer is used. All device structures of different gate combinations, varying channel thickness and oxide layers shown in figures 10(b), 10(c) and 10(d) exhibit identical drop of about 62% in saturation current. These plots establish that in the nanometer regime, interface fluctuation is the most prominent effect degrading device performance and reliability.

Gate characteristics of various device structures shown in figure 9 were used to calculate the threshold voltage(V_t) shift and subthreshold swing(s) variations from the smooth ideal interface device value. Figure 11(a) shows the variation of V_t and s with increase in κ of the oxide layer. The threshold voltage shift for rough device from the ideal device reduces markedly with increasing dielectric constant of the oxide layer. Similarly, the subthreshold swing approaches the ideal *60 mV/dec* value as the oxide dielectric constant is increased. The variation of V_t and s with the workfunction of the screen gate metal contact is shown in figure 11(b). As the screen gate workfunction increases, the shift of V_t and s from their ideal smooth surface values decrease. Therefore it is clear that better device performance stability against surface variations is achieved for a LCTM DG MOSFET with TaSiN-Al-TaSiN gates having high-κ Ta_2O_5 oxide layer.

6 Conclusion

This paper discussed the effect of surface roughness on the device performance of DG MOSFETs and compared that with the performance of the structurally modified LCTM DG MOSFET. A roughness point at the interface below the control gate has the largest effect in altering the ideal performance of the smooth interface device. Body thickness fluctuations caused by the interface roughness alter the potential profile and electron concentration in the channel to such an extent that it is the most important reason causing the fluctuations in device parameters. The roughness points near the control gate where the oxide layer protrudes into the Si channel cause the largest variation in device parameters from the smooth ideal interface value. The device characteristics such as the threshold voltage and the subthreshold swing vary appreciably from the ideal value due to the presence of roughness at the interface. The interface roughness is one of the most important reasons for the device performance fluctuations challenging the downscaling process. The structurally modified LCTM DG MOSFETs possess superior downscaling capabilities and better immunity to device performance fluctuations arising from interface roughness when compared with normal gate DG MOSFET with the same degree of roughness.

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